Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (canceled)

2. (currently amended) A capacitor for an integrated circuit comprising:

a first MOS-on-NWELL (Metal Oxide Semiconductor-on-N-doped well) device formed on a substrate and having a first pickup terminal and a first gate;

a second MOS-on-NWELL device formed on the substrate and having a second pickup terminal and a second gate,

wherein the first gate is connected to the second pickup terminal, and

wherein the second gate is connected to the first pickup terminal; ~~The capacitor of claim 1, further comprising:~~

a first PMOS (P-channel Metal Oxide Semiconductor Field Effect) transistor formed on the substrate and having its source and drain terminals connected together; and

a second PMOS transistor formed on the substrate and having its source and drain terminals connected together,

wherein a gate of the first PMOS transistor is connected to the source and drain terminals of the second PMOS transistor,

wherein a gate of the second PMOS transistor is connected to the source and drain terminals of the first PMOS transistor,

wherein the first gate, the second pickup terminal, the gate of the first PMOS transistor and the source and drain terminals of the second PMOS transistor are connected to a common terminal, and

wherein the second gate, the first pickup terminal, the gate of the second PMOS transistor and the source and drain terminals of the first PMOS transistor are connected to a second common terminal ~~and~~

~~wherein a combination of the first and second PMOS transistors are connected in parallel with the first and second MOS-on-NWELL devices~~.

3. (currently amended) A capacitor for an integrated circuit comprising:

a first PMOS (P-channel Metal Oxide Semiconductor Field Effect) transistor formed on a substrate and having its source and drain terminals connected together;

a second PMOS transistor formed on the substrate and having its source and drain terminals connected together,

wherein a gate of the first PMOS transistor is connected to the source and drain terminals of the second PMOS transistor, and

wherein a gate of the second PMOS transistor is connected to the source and drain terminals of the first PMOS transistor.

4. (currently amended) The capacitor of claim 3, further comprising:

a first MOS-on-NWELL (Metal Oxide Semiconductor-on-N-doped well) device formed on the substrate and having a first pickup terminal and a first gate;

a second MOS-on-NWELL device formed on the substrate and having a second pickup terminal and a second gate,

wherein the first gate is connected to the second pickup terminal, ~~and~~

wherein the second gate is connected to the first pickup terminal, ~~and~~

wherein the first gate, the second pickup terminal, the gate of the first PMOS transistor and the source and drain terminals of the second PMOS transistor are connected to a common terminal, and

wherein the second gate, the first pickup terminal, the gate of the second PMOS transistor and the source and drain terminals of the first PMOS transistor are connected to a second common terminal ~~wherein a combination of the first and second PMOS transistors are connected in parallel with the first and second MOS-on-NWELL devices~~.

5. (currently amended) A capacitor for an integrated circuit comprising:

a first plurality of MOS-on-NWELL (Metal Oxide Semiconductor-on-N-doped well) devices connected between a positive and a negative voltage to operate in an accumulation region as capacitors;

a second plurality of MOS-on-NWELL devices connected between the positive and the negative voltage to operate in a depletion region as capacitors;

a first plurality of PMOS (P-channel Metal Oxide Semiconductor Field Effect) transistors connected between the positive and the negative voltage to operate in an accumulation region as capacitors; and

a second plurality of PMOS transistors connected between the positive and the negative voltage to operate in a depletion region as capacitors.

6. (canceled)

7. (currently amended) A capacitor for an integrated circuit comprising:

a first MOS-on-PWELL (Metal Oxide Semiconductor-on-P-doped well) device formed on a substrate and having a first pickup terminal and a first gate;

a second MOS-on-PWELL device formed on the substrate and having a second pickup terminal and a second gate,

wherein the first gate is connected to the second pickup terminal, and

wherein the second gate is connected to the first pickup terminal; ~~The capacitor of claim 1, further comprising:~~

a first NMOS (N-channel Metal Oxide Semiconductor Field Effect) transistor formed on the substrate and having its source and drain terminals connected together; and

a second NMOS transistor formed on the substrate and having its source and drain terminals connected together,

wherein a gate of the first NMOS transistor is connected to the source and drain terminals of the second NMOS transistor,

wherein a gate of the second NMOS transistor is connected to the source and drain terminals of the first NMOS transistor,

wherein the first gate, the second pickup terminal, the gate of the first NMOS transistor and the source and drain terminals of the second NMOS transistor are connected to a common terminal, and

wherein the second gate, the first pickup terminal, the gate of the second NMOS transistor and the source and drain terminals of the first NMOS transistor are connected to a second common terminal ~~and~~

~~wherein a combination of the first and second NMOS transistors are connected in parallel with the first and second MOS-on-PWELL devices~~.

8. (currently amended) A capacitor for an integrated circuit comprising:

a first NMOS (N-channel Metal Oxide Semiconductor Field Effect) transistor formed on a substrate and having its source and drain terminals connected together;

a second NMOS transistor formed on the substrate and having its source and drain terminals connected together,

wherein a gate of the first NMOS transistor is connected to the source and drain terminals of the second NMOS transistor, and

wherein a gate of the second NMOS transistor is connected to the source and drain terminals of the first NMOS transistor.

9. (currently amended) The capacitor of claim [[3]] 8, further comprising:

a first MOS-on-PWELL (Metal Oxide Semiconductor-on-P-doped well) device formed on the substrate and having a first pickup terminal and a first gate;

a second MOS-on-PWELL device formed on the substrate and having a second pickup terminal and a second gate,

wherein the first gate is connected to the second pickup terminal, ~~and~~

wherein the second gate is connected to the first pickup terminal, ~~and~~

wherein the first gate, the second pickup terminal, the gate of the first NMOS transistor and the source and drain terminals of the second NMOS transistor are connected to a common terminal, and

wherein the second gate, the first pickup terminal, the gate of the second NMOS transistor and the source and drain terminals of the first NMOS transistor are connected to a second common terminal

~~wherein a combination of the first and second NMOS transistors are connected in parallel with the first and second MOS-on-PWELL devices.~~

10. (currently amended) A capacitor for an integrated circuit comprising:

a first plurality of MOS-on-PWELL (Metal Oxide Semiconductor-on-P-doped well) devices connected between a positive and a negative voltage to operate in an accumulation region as capacitors;

a second plurality of MOS-on-PWELL devices connected between the positive and the negative voltage to operate in a depletion region as capacitors;

a first plurality of NMOS (N-channel Metal Oxide Semiconductor Field Effect) transistors connected between the positive and the negative voltage to operate in an accumulation region as capacitors; and

a second plurality of NMOS transistors connected between the positive and the negative voltage to operate in a depletion region as capacitors.